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EXAMINER

NGUYEN, KEVIN M

ART UNIT PAPER NUMBER

2629

DATE MAILED: 08/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/038,501

Applicant(s)

SUNDAHL ET AL.

Examiner

Kevin M. Nguyen

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 08 June 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-24 and 31-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-24 and 31-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_.

***Response to Arguments***

1. Claims 25-30 are cancelled, the independent claims 1, 14 and 18 are not amended, the dependent claims 2, 6, 7, 15, 16, 17 19, 20 23 are amended, and the dependent claims 31-33 are newly added. Thus, claims 1-24 and 31-33 are currently pending in the application. Response to applicant's argument filed on 08 June 2006 has been fully considered, and is not persuasive. The rejections of claims 1-24 are maintained. Applicant's argument with respect to claims 31-33 has been fully considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Ju et al (US 5,497,258) hereinafter Ju.

4. It is respectfully submitted that in the case law stated "Drawing as a Reference", "Things clearly shown in reference patent drawing qualify as prior art features, even though unexplained by the specification". See *In re Mraz*, 173 USPQ 25 (CCPA 1972). "A claimed invention may be anticipated or rendered obvious by a drawing in a reference, whether the drawing disclosure by accidental or intentional. However, a

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reference, whether the drawing disclosure by accidental or intentional. However, a drawing is only available as a reference for what it would teach one skilled in the art who did not have the benefit of applicant's disclosure". See *In re Meng*, 181 USPQ 94, 97 (CCPA 1974). "Absent of any written description in the reference specification of quantitative values, arguments based on measurement of a drawing are of little value in proving anticipation of a particular length". See *In re Wright*, 193 USPQ 332, 335 (CCPA 1977).

5. As to claim 1, Figure 1 of Ju teaches a device for rendering an image, comprising:

an integral panel [a liquid crystal spatial light modulators (SLMs) panel 10 are integrated circuit into a single device, see col. 1, lines 18-22] having a viewing side [a cover glass 13, see Fig. 1, see col. 4, lines 27-30] that includes a front panel surface [an antireflective coating 28, see Fig. 1, col. 4, lines 29] and a non-viewing side [a substrate 11, see Fig. 1, col. 8, lines 52-55] that includes a rear panel surface opposed to and facing away from the front panel surface, said non-viewing side having:

Figure 5 of Ju further teaches a peripheral region formed on the rear panel surface [pads 37, solder joints 27, and four-sided wire bond path 19 are on the substrate 11, see col. 8, lines 12-15];

Figure 5 of Ju further teaches a central region formed on the rear panel surface [VLSI chip 12, see col. 8, lines 15-25];

Figures 1 and 5 of Ju further teach a pattern of contacts [solder pads 25, 26 36 of VLSI chip 12] exposed to the rear panel surface formed in the central region of the non-viewing side [see col. 8, lines 46-59].

As to claim 2, Ju teaches wherein the pattern of contacts is configured to electrically connect a component to the viewing device [the solder pads 25, 26, 36 of VLSI chip 12, see Figs. 1 and 5, wires or wire bonds 19 are provided on all four sides of VLSI chip 12 to connect the individual pixel circuits of chip 12 to the circuit path that are carried by substrate 11, see col. 4, lines 62-65].

As to claim 3, Ju teaches wherein the component is a printed circuit board [the substrate member 11 is a silicon wafer having a plated wire pattern on the upper surface thereof, see col. 4, lines 22-24].

As to claim 4, Ju teaches wherein the component is an integrated circuit [the Very Large Scale Integration (VLSI) chip 12, see Fig. 5, the abstract, and the title].

As to claim 5, Ju teaches wherein the component is a view device driver circuit [a driver D drives the VLSI's metal crystal modulating pad, LC pad 45 of Fig. 7, see col. 7, lines 32-38].

As to claim 6, Ju teaches further comprising a socket electrically coupled to the pattern of contacts and structured to receive and electrically connect a component in the central zone [the VLSI chip 12 inherent has a plurality of pins that receives into which the substrate 11 can be inserted, see Fig. 1, and the abstract, lines 5-10].

As to claim 7, Fig. 5 of Ju teaches wherein the pattern of contacts is configured to electrically connect a plurality of components to the viewing device [the VLSI 12 has

the pattern of contacts corresponding to the solder pads 25, 26, 36 to the SLM display panel 10, see Figs. 1 and 5].

As to claim 8, Fig. 5 of Ju teaches further comprising a plurality of components connected to the non-viewing side of the panel [two or more VLSI chip 12 are accurately located relative to a single underlying substrate member 11, see col. 9, lines 35-38].

As to claim 9, Ju teaches further comprising a display contact layer [the LD pads 45 also act a pixel reflectors for the liquid crystal layer, see col. 7, lines 45-46], a dielectric layer [the glass 13, see col. 8, line 64], and an electrically conductive circuit layer including the pattern of contacts [the VLSI 12 has the pattern of contacts corresponding to the solder pads 25, 26, 36, see Fig. 5].

As to claim 10, Ju teaches wherein the display contact layer couples the plurality of display cells and the electrically conductive circuit layer [the LD pads 45 also act a pixel reflectors for the liquid crystal layer, the VLSI 12 has the pattern of contacts corresponding to the solder pads 25, 26, 36 that contacts the LD pads 45 , see col. 7, lines 50-53].

6. As to claim 11, Ju teaches wherein the electrically conductive circuit layer couples the display contact layer and the bond pad [FIG. 7 is a top view of VLSI chip 12 in FIG. 1, showing the pixel arrangement of LC pads 45 to each of which a circuit of FIG. 3 is connected, see col. 7, lines 50-53].

As to claim 12, Ju teaches wherein the bond pad layer includes a plurality of bond pads operative to couple the electrically conductive circuit layer to an attached component [the LD pads 45 also act a pixel reflectors for the liquid crystal layer, the

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VLSI 12 has the pattern of contacts corresponding to the solder pads 25, 26, 36 that contacts the LD pads 45 , see col. 7, lines 50-53].

As to claim 13, Ju teaches wherein the bond pad layer includes a plurality of bond pads operative to couple the electrically conductive circuit layer to an attached plurality of components [the LD pads 45 also act a pixel reflectors for the liquid crystal layer, the VLSI 12 has the pattern of contacts corresponding to the solder pads 25, 26, 36 that contacts the LD pads 45 , see col. 7, lines 50-53; two or more VLSI chip 12 are accurately located relative to a single underlying substrate member 11, see col. 9, lines 35-38].

7. As to claim 14, Ju teaches a viewing device, comprising:

a panel [a spatial light modulators (SLMs) panel 10, see Fig. 1] including:

a plurality of display cells [a plurality of pixels, see Fig. 3, col. 7, lines 17-22] distributed on the first side of the panel [a cover glass 13, see Fig. 1], the display cells [the plurality of pixels] configured to display an image [a visual image, see col. 2, lines 61-65] that is viewable on a front panel surface formed on the first panel side [the cover glass 13];

a rear surface [a substrate member 11, see Fig. 1] opposed to a facing away from the front panel surface, the rear panel surface formed on a second side of the panel;

a central zone [element 12, see Fig. 5] and a peripheral zone [elements 37/27, see Fig. 5] formed on the rear panel surface [the substrate member 11, see fig. 1];

a matrix of interconnects exposed to the rear panel surface, the matrix of interconnects structured to connect a component to the rear panel surface in the central zone [the solder pads 25, 26, 36 of VLSI chip 12, see Figs. 1 and 5, wires or wire bonds 19 are provided on all four sides of VLSI chip 12 to connect the individual pixel circuits of chip 12 to the circuit path that are carried by substrate 11, see col. 4, lines 62-65].

8. As to claim 15, Ju discloses wherein the matrix of interconnects [36/35, fig. 6] is configured to electrically connect [electrical wire connection 19, fig. 1] a plurality of components [11, 12] to the viewing device [10].

9. Claim 16 shares the same limitations as those of claim 15 and therefore the rationale for rejection will be the same.

10. Claim 17 shares the same limitations as those of claim 6 and therefore the rationale for rejection will be the same.

11. As to claim 18, Ju teaches an electronic display system, comprising:

an image generator [the voltage on the data line is passed to the input capacitance of driver D, see Fig. 3, col. 7, lines 35-37];

a display interface coupled to the image generator [the driver D drives, or charges, the VLSI's metal crystal modulating LC pad 45 of Fig. 7, see col. 7, lines 37-38];

a display coupled to the display interface [LC pads, see col. 7, lines 50-53], the display including:

a panel [the SLMs panel 10, fig. 1] having a first side [a cover glass 13] and a second side [a substrate 11], the first side of the panel including a plurality



of display cells distributed thereon [a plurality of pixels, see col. 7, line 22], the plurality of display cells structured to display an image [a visual image, see col. 2, line 62] that is viewable from the first side of the panel, the second side of the panel being opposed to and facing away from the first side of the panel [the substrate 11, see Fig. 1];

a matrix of interconnects exposed to a surface formed on the second side of the panel, the matrix of interconnects structured to connect a component to the second side of panel [the solder pads 25, 26, 36 of VLSI chip 12, see Figs. 1 and 5, wires or wire bonds 19 are provided on all four sides of VLSI chip 12 to connect the individual pixel circuits of chip 12 to the circuit path that are carried by substrate 11, see col. 4, lines 62-65].

12. As to claim 19, Fig. 5 of Ju teaches wherein the panel further includes a periphery and the component is connected to the panel within the periphery [pads 37, solder joints 27, and four-sided wire bond path 19 are on the substrate 11, see col. 8, lines 12-15].

13. As to claim 20, Fig. 5 of Ju teaches wherein a plurality of components are electrically connected to the panel within the periphery [pads 37, solder joints 27, and four-sided wire bond path 19 are on the substrate 11, see col. 8, lines 12-15].

14. Claim 21 shares the same limitations as those of claim 3 and therefore the rationale for rejection will be the same.

15. Claim 22 shares the same limitations as those of claim 4 and therefore the rationale for rejection will be the same.

16. Claim 23 shares the same limitations as those of claim 6 and therefore the rationale for rejection will be the same.

17. As to claim 24, Fig. 1 of Ju teaches further comprising a video driver [the drive D, the VLSI chip 12] interposed between the display interface [LC layer 16] and the matrix of interconnects [pads 37, solder joints 27, and four-sided wire bond path 19].

***Claim Rejections - 35 USC § 103***

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

19. Claims 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ju in view of Yoshimura et al (US 6,847,415) hereinafter Yoshimura.

20. As to claim 31, Ju teaches all of the claimed limitation of claim 1, except for “wherein the circuit board is opposite a portion of the front panel surface on which the image is viewable and wherein the pattern of contacts is structured to electrically connect a component to the viewing device.

However, figure 6D of Yoshimura discloses a third embodiment of a flat display unit 1 which includes a circuit board 4 are secured to a rear surface of chassis 2, opposite to recess 2b having a display panel 3 adhered thereto, see col. 8, lines 51-54, and col. 10, lines 59-66 for further details of the explanation.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the Ju's reference to become the circuit board 4 are

secured to the rear surface of chassis 2, opposite to recess 2b having the display panel 3 adhered thereto as taught by Yoshimura in order to achieve the benefit of improving an excellent heat dissipation efficiency by virtue of its larger surface area compared with that of display panel 3, while fabricating a flat display panel at low cost, and being free from the damages during tests and inspections without using a protector [see Yoshimura, col. 3, lines 10-12, col. 6, lines 8-11, and col. 10, lines 30-31].

21. As to claim 32, the combination of figure 4 of Ju and figure 5E of Yoshimura discloses wherein the central region [the chip 12 of Ju is placed at a center] is opposite a portion of the front panel surface [33 of Yoshimura] on which the image is viewable and wherein the matrix of interconnects is structured to electrically connect [a flexible cable 35 of Yoshimura] a component to the viewing device [31 of Yoshimura].

22. As to claim 33, the combination of Ju and Yoshimura discloses wherein the surface on which the matrix of interconnects [36/35 of Fig. 6 of Ju] is exposed is opposite a portion of the display cells on which the image is displayable and wherein the matrix of interconnects is structured to electrically connect a component to the display [fig. 5E of Yoshimura].

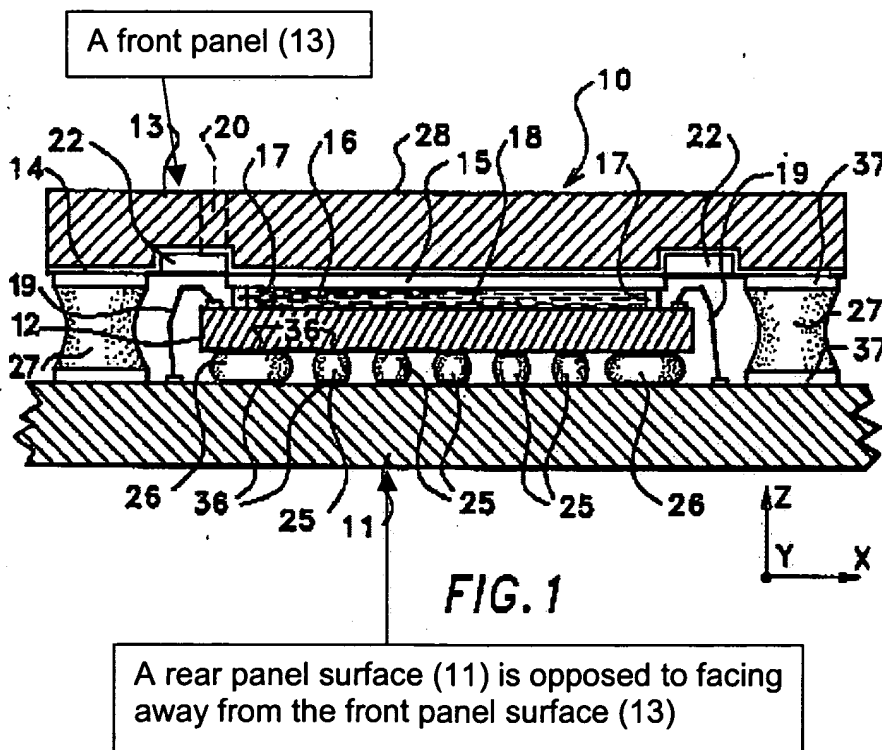
### ***Response to Arguments***

23. Applicant's arguments filed 08 June 2006 have been fully considered but they are not persuasive.

24. Applicant argues that claims 1, 14 and 18 recite "an integral panel having a viewing side that includes a front panel surface and a non-viewing side that includes a rear panel surface opposed to and facing away from the front panel surface," see

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remarks at page 6. In response, the examiner respectfully disagrees. As stated *supra* with respect to claims 1, 14, and 18, the examiner indicated that the broad claimed limitation “an integral panel having a viewing side that includes a front panel surface and a non-viewing side” still meets by Ju’s reference. Furthermore, Ju further discloses fig. 1 is a cross-section side view of a VLSI SLM 10 [see col. 4, lines 15-16]. The term VLSI stands for very-large-scale integration is the process of creating integrated circuits by combining thousands of transistor-based circuits into on a single chip<sup>1</sup>. Thus, the integrated circuits SLM 10 corresponds to the integral panel as claimed.



25. Applicant argues with respect to claim 1, 14, and 18 Ju does not teach the rear panel surface points in the same direction as the front panel surface—not “opposed to

<sup>1</sup> See [http://en.wikipedia.org/wiki/Very-large-scale\\_integration](http://en.wikipedia.org/wiki/Very-large-scale_integration) for more details.

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disagrees. Figure 1<sup>2</sup> of Ju as indicated above further still meets said broad claimed limitation “opposed to and facing away”.

26. In response to applicant's argument that “opposed to and facing away,” a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

27. Applicant argues the rear panel surface having the vectors extend perpendicularly in the same direction as the front panel surface. In response, the examiner respectfully disagrees because the applicant's argument is nothing to be related to the claimed invention. Furthermore, the vectors of Ju is indicated a structure of the display panel in three dimensions X, Y, and Z.

28. Applicant argue Ju's pads 36 and solder points 25, 26 do not make electrical connections. In response, the examiner respectfully disagrees because Ju discloses a wire 19 is used to connect (or electrically connect) the circuits of VLSI<sup>1</sup> chip 12, see col. 8, lines 13-25 for further details of the explanation. The technical term “electrically connect” is very well known in the circuit of VSLI chip. Thus, the rejection 102 is proper.

29. In response to applicant's argument that “contact or interconnects for making electrical connections to be exposed to the rear panel surface opposite to where the image is viewable,” a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to

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<sup>2</sup> See Drawing as a reference at paragraph 4 above.

patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

30. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

31. Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections.

For these reasons, the rejections based on Ju and Yoshimura have been maintained.

32. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. NGUYEN whose telephone number is 571-272-7697. The examiner can normally be reached on MON-THU from 8:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, a supervisor RICHARD A. HJERPE can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the Patent Application Information Retrieval system, see <http://portal.uspto.gov/external/portal/pair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KMN  
July 26, 2006

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Patent Examiner  
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